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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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06/22/2004

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EXAMINER

PHAM, LY D

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/785,556

Applicant(s)

ROOHPARAR ET AL.

Examiner

Ly D Pham

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 0204.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. Applicant's Information Disclosure Statement, IDS, has been considered by the examiner.
2. Claims 1 – 20 are presented for the examination.

#### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 2, 3, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat 6,324,602 B1) in view of Silverbrook (US Pat Pub 2002/0071104 A1).

Regarding **claim 1**, Chen et al. disclose a non-volatile memory device (col. 4, lines 42 – 52, non-volatile random access memory, NVRAM) comprising:

an array of non-volatile memory cells (fig. 1, 16), wherein the array comprises bit lines coupled to the non-volatile memory cells (bit lines coupled to memory cells for passing data in and out of memory cells are inherent. See also col. 4, line 63 – col. 5, line 5);

sense amplifier circuitry coupled to the bit lines (col. 5, lines 13 – 17), wherein the sense amplifier circuitry detects a differential voltage between the bit lines (col. 12, lines 8 – 14);

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal (col. 6, lines 36 – 41).

Although Chen et al. did not clearly incorporate the Rambus DRAM I/O interface technology to the disclosure, such I/O architecture has however been considered well known to the industry (col. 1, line 65 – col. 2, line 5). Nevertheless, the combination of Rambus interconnect configuration to NVRAM has been shown by Silverbrook (paragraph 0450, “a 4Mbyte Flash memory 70 for program storage ..., direct RAMbus interface 81, ...). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made to incorporate the Rambus interconnect technology to the non-volatile I/O interface as shown by Chen et al., so that rows, columns, and data buses are multiplexed for increased data rate (Chen et al., col. 2, lines 8 – 9. See also col. 9, lines 15 – 18, and col. 13, line 26 – col. 14, line 67, multiplexed data signal implemented in the memory device).

Regarding **claim 2**, Chen et al. also disclose the memory device of claim 1, further comprising input circuitry to receive input data connection on rising and falling edges of the clock signal (col. 9, lines 20 – 23, I/O interface at DDR ...).

Regarding **claim 3**, Chen et al. also disclose the memory device of claim 1, wherein the array of non-volatile memory cells is arranged in a plurality of addressable blocks (col. 5, lines 2 – 6, blocks and banks are equivalent in memory arts).

Regarding **claim 7**, Chen et al. also disclose the memory device of claim 1, wherein the bit lines are pre-charged to different voltage levels prior to accessing a memory cell (col. 11, lines 18 – 21 and col. 12, lines 8 – 14, sense amp enabled after differential voltages established).

Art Unit: 2818

5. Claims 5, 6, and 8 – 12, and 15 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat 6,324,602 B1), Silverbrook (US Pat Pub 2002/0071104 A1), and further in view of Deneroff et al. (US Pat 6,215,686 B1).

Regarding **claims 5 and 6**, although Chen et al. and Silverbrook did not clearly show the memory further adapted to provide burst oriented read accesses wherein the output data start at a selected location and continue for a programmed number of locations in a programmed sequence. However, this has been shown by Deneroff et al. (col. 10, lines 61 – 67). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature shown by Deneroff et al. to the disclosures by Chen et al. and Silverbrook, so that read and write access to memory components can be controlled (col. 11, lines 33 – 50).

**Claims 8 and 12** are rejected on grounds of rejection of claims 1, 5, and 6. Chen et al. disclose a processor for a processing system as claimed in claim 12 (col. 2, lines 29 – 31).

**Claims 9 and 14** are rejected on grounds of rejection of claim 7, wherein active digit line pre-charged to a voltage greater than a complementary digit line is equivalent to the digit lines pre-charged to different voltage levels prior to access operations.

Regarding **claims 11 and 19**, Chen et al. further disclose the flash memory of claim 8, wherein the pre-charge circuitry pre-charges the digit lines to a differential level using a bias circuit (fig. 7, pre-charge circuit 64 is supplied with bias circuit which generates the bias  $V_{pc}$ ).

Regarding **claims 10 and 19**, the examiner takes an Official Notice of the claimed feature, wherein the pre-charge circuitry pre-charges the digit lines to a differential level using charge sharing, to be considered common and well-known to one skilled in the art, for achieving improved access time.

Art Unit: 2818

Regarding **claim 15**, the examiner takes an Official Notice to the claimed feature, wherein the processor is adapted to receive burst transmissions of data from the memory device, to be considered well known to one of skilled in the art, for which the processor initiate a burst read operation from non-volatile memory without incurring wait states after a number of initial wait states.

Regarding **claims 16 – 18**, it is considered inherent in memory art where flash memory is non-volatile, which comprises floating gates; and system processor generates system commands.

6. Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al., Silverbrook, Deneroff et al., and further in view of Mills et al. (US Pat 6,385,688 B1).

Regarding **claim 15**, Mills et al. show the processor adapted to receive burst transmissions of data from the memory device (col. 19, lines 42 – 46). Therefore, it is considered obvious to one of ordinary skill in the art, to include the processor with such capability to the system shown by Chen et al., etc..., to allow a multiple-burst access of indeterminate length to occur at highest system performance (col. 19, lines 56 – 58).

Regarding **claim 20**, Mills et al. further show the system of claim 12, further including a unified communication bus coupling the processor with the RDRAM compatible non-volatile memory device and volatile memory device (fig. 13, microprocessor 1310 coupled to flash 1350 and volatile DRAM 1360 through unified communication bus 1320).

### ***Double Patenting***

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

Art Unit: 2818

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. **Claims 1 – 6 and 8** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 5 of U.S. Patent No. 6,741,497 B2.

Although the conflicting claims are not identical, they are not patentably distinct from each other because each and every limitation claimed in claims 1 – 6 and 8 have been previously disclosed and patented.

### ***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

Art Unit: 2818

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

12. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is **571-272-1793**. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at **571-272-1787**. The fax number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Ly Pham



June 18, 2004



**David Nelms**  
Supervisory Patent Examiner  
Technology Center 2800